CLAIMS

What is claimed is:

We claim:

1. A method, comprising:

determining a bootstrap processor from a plurality of operable processors in a fault tolerant multiprocessor system irrespective of an initialization time of a particular operable processor.

2. The method of claim 1, further comprising:

asserting a first signal;

asserting a second signal; and

ensuring that both the first signal and the second signal are asserted prior to allowing the plurality of operable processors to enter a bootstrap processor arbitration process.

3. The method of claim 2, wherein the first signal indicates that a particular processor has successfully completed an initialization sequence, and the second signal indicates that all of the operable processors in the fault tolerant multiprocessor system are ready to enter the bootstrap processor arbitration process.

4. The method of claim 2, wherein the second signal is communicated across the system bus to each processor.

5. The method of claim 2, wherein asserting is selected from one in a group consisting of driving a signal line to a logical 0, driving the signal line to a logical 1, toggling the signal line from a logical 1 to a logical 0, and driving the system bus to a logic state on a first clock cycle and releasing the system bus on a second clock cycle.

6. The method of claim 1, wherein the fault tolerant multiprocessor system comprises a multiprocessor system which continues to be operable irrespective of a fault occurring in any particular processor.

7. The method of claim 1, wherein the operable processor comprises a processor which has successfully completed an initialization and testing sequence.

8. A method, comprising:

using a system bus to initiate a bootstrap processor arbitration process in a system containing a plurality of operable processors; and

stalling transactional activity on the system bus until all of the plurality of operable processors are ready to enter the bootstrap processor arbitration process.

9. The method of claim 8, further comprising:

electing one of the plurality of operable processors as the bootstrap processor.

10. The method of claim 8, wherein a bus controller stalls transactional activity on the system bus until the bootstrap processor determination has been made.

11. The method of claim 9, wherein the electing of the bootstrap processor includes the steps of:

sending a first control signal to a first processor designating the first processor as the bootstrap processor;

checking that the first processor is operable;

if the first processor is not operable, then sending a second control signal to a second processor designating the second processor as the bootstrap processor;

checking that the second processor is operable; and

if the second processor is not operable, then repeating the above steps for each successive processor until an operable bootstrap processor is designated.

12. The method of claim 9, wherein the electing of the bootstrap processor includes the steps of:

sending a first control signal to a plurality of processors designating the arbitration identification numbers of each particular processor;

sequencing through the plurality processors until an operable processor is found; and

designating the operable processor as the bootstrap processor.

13. A computing system, comprising:

a plurality of operable processors;

a system bus; and

an arbitration protocol to determine a bootstrap processor from the plurality of operable processors in a fault tolerant multiprocessor system irrespective of an initialization time of a particular operable processor.

14. The computing system of claim 13, wherein the arbitration protocol comprises micro code instructions.

15. The computing system of claim 13, wherein the arbitration protocol comprises logic circuitry located in a processor.

16. The computing system of claim 13, wherein the arbitration protocol conducts the bootstrap processor arbitration process across the system bus.

17. The computing system of claim 13, wherein each of the operable processors has a bus controller, the bus controller to stall transactional activity on the system bus until the bootstrap processor determination has been made.

18. An apparatus, comprising:

a computer readable media; and

instructions embedded on the computer readable media, the instructions when executed by a machine, cause the machine to perform operations comprising:

determine a bootstrap processor from a plurality of operable processors in a fault tolerant multiprocessor system irrespective of an initialization time of a particular operable processor.

19. The apparatus of claim 18, further comprising instructions, which when executed by the machine, cause the machine to perform operations comprising:

to assert a first signal;

to assert a second signal; and

to ensure that both the first signal and the second signal are asserted prior to allowing the plurality of operable processors to enter a bootstrap processor arbitration process.

20. The apparatus of claim 19, wherein the first signal indicates that a particular processor has successfully completed an initialization sequence, and the second signal indicates that all of the operable processors in the fault tolerant multiprocessor system are ready to enter the bootstrap processor arbitration process.

21. The apparatus of claim 19, wherein the first signal indicates that a particular processor has been assigned an arbitration identification number.

22. The apparatus of claim 19 wherein the instructions comprise micro code.

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